

1 What is claimed is:

- 2
- 3 1. A method of designing digital signal processing hardware to implement a z-
- 4 domain transfer function, wherein the processing of signal samples is
- 5 characterized by constant latency, the method comprising:
- 6     a) specifying said transfer function;
- 7     b) without regard to latency characteristics, specifying a first hardware stage
- 8         to process said signal samples in accordance with said transfer function;
- 9         and
- 10     c) specifying a second hardware stage to dynamically selectively delay said
- 11         signal samples processed by said first hardware stage such that the
- 12         combined first and second stage latency for the processing of said signal
- 13         samples is a constant.
- 14
- 15 2. The method of designing digital signal processing hardware of claim 1, wherein
- 16         said first hardware stage is a generic data processor.
- 17
- 18 3. The method of designing digital signal processing hardware of claim 1, wherein
- 19         said second hardware stage includes a multistage FIFO.
- 20
- 21 4. The method of designing digital signal processing hardware of claim 1, wherein
- 22         said second stage includes a selector that couples to the second stage output a
- 23         selected one of a plurality of sequentially delayed variations of the samples
- 24         provided to the second stage input.

- 1       5. The method of designing digital signal processing hardware of claim 4, wherein  
2           the selector control is a function of shifts into and out of said first stage.  
3  
4       6. The method of designing digital signal processing hardware of claim 4, wherein  
5           the selector control includes an up/down counter.  
6  
7       7. The method of designing digital signal processing hardware of claim 1, further  
8           including:  
9              independent of said specifying of said first hardware stage, specifying the  
10             target implementation technology.  
11  
12      8. The method of designing digital signal processing hardware of claim 7, wherein  
13           the target implementation technology is a design approach selected from the group  
14           consisting of FPGA, ASIC, semi-custom, and custom.  
15  
16      9. The method of designing digital signal processing hardware of claim1, further  
17           including:  
18              independent of said specifying of said first hardware stage, specifying the  
19             target arithmetic library.

20  
21

1        10. The method of designing digital signal processing hardware of claim 1, further  
2        including:  
3            a) specifying a first technology as the target implementation technology; and  
4            b) after said specifying of said target implementation technology and said  
5              specifying of said first hardware stage, and without requiring modification  
6              of the specification of said first hardware stage, changing the target  
7              implementation technology to a second technology.

8  
9        11. The method of designing digital signal processing hardware of claim 1, further

10      including:  
11            a) specifying a test bench for the testing of the transfer function, said test  
12              bench including simulation modules and test vectors, said transfer function  
13              being conceptually modeled as being of the form  $z^N \times T(z)$ , where  $T(z)$  is  
14              the desired transfer function and where the realization of the  $z^{-N}$  delay may  
15              be configured independent of other aspects of the test bench;  
16            b) specifying a first technology as the target implementation technology and  
17              specifying the  $z^{-N}$  delay based on the target implementation technology;  
18            c) after said specifying of said first hardware stage, said test bench, said  
19              target implementation technology, and said  $z^{-N}$  delay, changing the target  
20              implementation technology to a second technology without requiring  
21              revised specification of said first hardware stage and without requiring  
22              modification of said test bench beyond the revised specification of said  $z^{-N}$   
23              delay in accordance with the second technology.

24

1       12. The method of designing digital signal processing hardware of claim 1, further  
2       including:  
3           a) specifying a first library as the target arithmetic library; and  
4           b) after said specifying of said first library and said specifying of said first  
5           hardware stage, and without requiring modification of the specification of  
6           said first hardware stage, changing the target arithmetic library to a second  
7           library.

8

9       13. The method of designing digital signal processing hardware of claim 1, further

10      including:  
11           a) specifying a test bench for the testing of the transfer function, said test  
12           bench including simulation modules and test vectors, said transfer function  
13           being conceptually modeled as being of the form  $z^N \times T(z)$ , where  $T(z)$  is  
14           the desired transfer function and where the realization of the  $z^{-N}$  delay may  
15           be configured independent of other aspects of the test bench;  
16           b) specifying a first library as the target arithmetic library and specifying the  
17            $z^{-N}$  delay based on the target arithmetic library;  
18           c) after said specifying of said first hardware stage, said test bench, said  
19           target arithmetic library, and said  $z^{-N}$  delay, changing the target arithmetic  
20           library to a second library without requiring revised specification of said  
21           first hardware stage and without requiring modification of said test bench  
22           beyond the revised specification of said  $z^{-N}$  delay in accordance with the  
23           second library.

1      14. A method of operating digital signal processing hardware to implement a z-  
2      domain transfer function, wherein the processing of signal samples is  
3      characterized by constant latency, the method comprising:  
4            a) providing a first and second hardware stage;  
5            b) configuring and operating said first hardware stage to process said signal  
6                samples in accordance with said transfer function, said first hardware stage  
7                processing said signal samples with variable latency; and  
8            c) operating said second hardware stage to dynamically selectively delay said  
9                signal samples processed by said first hardware stage such that the  
10               combined first and second stage latency for the processing of said signal  
11               samples is a constant.

12

13      15. The method of operating digital signal processing hardware of claim 14, wherein  
14               said first hardware stage is a generic data processor.

15

16      16. The method of operating digital signal processing hardware of claim 14, wherein  
17               said second hardware stage includes a multistage FIFO.

18

19      17. The method of operating digital signal processing hardware of claim 14, wherein  
20               said second stage includes a selector that couples to the second stage output a  
21               selected one of a plurality of sequentially delayed variations of the samples  
22               provided to the second stage input.

1       18. The method of operating digital signal processing hardware of claim 17, wherein  
2           the selector control is a function of shifts into and out of said first stage.

3

4       19. The method of operating digital signal processing hardware of claim 17, wherein  
5           the selector control includes an up/down counter.

6

7       20. Circuitry for implementing a z-domain transfer function for the processing of  
8           signal samples, the circuitry comprising:

9           a) transfer function circuitry, said transfer function circuitry processing said  
10              signal samples in a first variable length pipeline in accordance with said  
11              transfer function, said transfer function circuitry processing V samples at  
12              any given time;

13           b) delay circuitry following said transfer function circuitry, said delay  
14              circuitry delaying in a second variable length pipeline signal samples  
15              processed previously by said transfer function circuitry, said delay  
16              circuitry delaying D of samples at any given time; and

17           c) delay circuitry control logic coupled to said transfer function circuitry and  
18              said delay circuitry and dynamically adjusting the number of said D  
19              samples to maintain the sum of V and D as a constant.

20

21       21. The circuitry for implementing a z-domain transfer-function of claim 20, wherein  
22           said transfer function circuitry includes a generic data processor.

23

1        22. The circuitry for implementing a z-domain transfer function of claim 20, wherein  
2            said second delay circuitry includes a multistage FIFO.

3

4        23. The circuitry for implementing a z-domain transfer function of claim 20, wherein  
5            said delay circuitry includes a selector that couples to the delay circuitry output a  
6            selected one of a plurality of sequentially delayed variations of the samples  
7            provided to the delay circuitry input.

8

9        24. The circuitry for implementing a z-domain transfer function of claim 23, wherein  
10           the delay circuitry control is a function of shifts into and out of said transfer  
11           function circuitry.

12

13        25. The circuitry for implementing a z-domain transfer function of claim 23, wherein  
14           the delay circuitry control includes an up/down counter.

15

16

1    26. A digital signal processing building block for processing block-input signal  
2    samples to create block-output signal samples in accordance with the closed-loop  
3    z-domain transfer function  $A(z)/(1+A(z))$ , where  $A(z)$  is an open-loop transfer  
4    function, the building block comprising:

- 5    a)  $B(z)$  transfer function circuitry having a  $B(z)$ -input and a  $B(z)$ -output, said  
6     $B(z)$  transfer function circuitry processing signal samples received at the  
7     $B(z)$ -input in a first variable length pipeline in accordance with a  $B(z)$   
8    transfer function, said  $B(z)$  transfer function circuitry processing  $V$  signal  
9    samples at any given time;
- 10   b)  $D(z)$  delay circuitry following said  $B(z)$  transfer function circuitry,  
11   wherein  $A(z) = B(z) \times D(z)$ , said  $D(z)$  delay circuitry delaying in a second  
12   variable length pipeline samples received from said  $B(z)$ -output, the delay  
13   circuitry delaying  $D$  signal samples at any given time before providing  
14   them as the block-output signal samples;
- 15   c)  $D(z)$  delay circuitry control logic coupled to said  $B(z)$  transfer function  
16   circuitry and said  $D(z)$  delay circuitry and dynamically adjusting the  
17   pipeline length of  $D(z)$  to maintain the sum of  $V$  and  $D$  as a constant;
- 18   d) a summer having a positive input, a negative input, and a difference  
19   output, said positive input receiving block-input signal samples, said  
20   negative input receiving said block-output signal samples, said difference  
21   output providing difference signal samples to the  $B(z)$ -input.

22  
23   27. The digital signal processing building block of claim 26, wherein said  $B(z)$  transfer  
24   function circuitry includes a generic data processor.  
25

1    28. The digital signal processing building block of claim 26, wherein said D(z) delay  
2    circuitry includes a multistage FIFO.

3

4    29. The digital signal processing building block of claim 26, wherein said D(z) delay  
5    circuitry includes a selector that couples to the block-output a selected one of a  
6    plurality of sequentially delayed variations of the samples provided by the B(z)-  
7    output.

8

9    30. The digital signal processing building block of claim 26, wherein the D(z) delay  
10   circuitry control is a function of shifts into and out of said B(z) transfer function  
11   circuitry.

12

13   31. The digital signal processing building block of claim 26, wherein the D(z) delay  
14   circuitry control includes an up/down counter.

15